/789421.sch
Message 9:
From spo_patent@spo.eds.com Thu Aug 7 10:00:29 1997
Received: from pin1.spo.eds.com (www.spo.eds.com [192.238.49.35]) by pioneer.uspto.gov (8.7.4/8.7.3) with SMTP id KAA22695 for <mayasyst@pioneer.uspto.gov>; Thu, 7 Aug 1997 10:00:27 -0400 (EDT)
From: spo_patent@spo.eds.com
Received: by pin1.spo.eds.com (4.1/spo-1.5)
id AA13149; Thu, 7 Aug 97 08:58:51 CDT
Received: from spo.spo.eds.com by spo1.eds.com (4.1/SPOUUCP-1.8)
id AA02315; Thu, 7 Aug 97 08:52:20 CDT
Received: from spo4.spo.eds.com by spo.spo.eds.com (4.1/SPO-2.5)
id AA13778; Thu, 7 Aug 97 08:52:18 CDT
Date: Thu, 7 Aug 97 08:52:17 CDT
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To: mayasyst@pioneer.uspto.gov
Sender: spo_patent@spo.eds.com
Subject: Re: 789421.sch
X-Mailer: SPO Mail
Mime-Version: 1.0
Message-Id: <19970807_084417_spo_13484>
Content-Type: text/plain; charset=us-ascii
Status: RO

CUSTOMER REQUEST SUMMARY

Your request was:

>e003
>
>Word frequency list for document 789421
>
>---search-id---
>789421, hua ly
>---search-id---
>
>---word freq---

> 1 ability	1 accessed	1 accompanying
> 1 accomplished	5 according	1 accordingly
> 1 active	1 activity	2 adapted
> 2 additional	2 additionally	1 address
> 1 addressable	2 addressed	1 adequately
> 1 advantage	1 advantages	3 after
> 1 aging	4 all	6 allows
> 1 alone	4 also	2 among
> 1 amounts	29 and	14 another
> 4 any	1 application	1 applications
> 1 architecture	20 are	1 arising
> 1 array	1 art	1 ash
> 4 aspect	1 aspects	1 attempt
> 1 automatically	1 back	1 background
> 1 bad	1 become	1 becomes
> 1 becoming	1 being	1 beprom
> 1 block	1 bulky	5 bus
> 1 but	10 cache	5 can

> 8 card
> 18 cells
> 4 circuit
> 2 codes
> 1 commands
> 2 comprising
> 1 connectable
> 2 consequently
> 1 contain
> 1 control
> 1 conventional
> 1 correctly
> 1 cycling
> 4 defect
> 1 deselected
> 1 determining
> 1 disadvantageous
> 1 down
> 2 drive
> 4 each
> 1 eepront
> 1 electrically
> 1 emulating
> 1 endure
> 2 erasable
> 4 erasing
> 1 even
> 1 expensive
> 1 features
> 2 files
> 24 flash
> 10 from
> 1 generally
> 1 good
> 2 have
> 2 important
> 2 improvements
> 4 including
> 1 increase
> 1 inducing
> 1 instead
> 1 interface
> 24 invention
> 5 its
> 1 levels
> 1 long
> 1 maintaining
> 1 many
> 1 mass
> 1 mechanical
> 1 minimize
> 5 more
> 2 mounted
> 1 multiple

1 cards
3 chip
3 circuits
5 combination
1 communicate
7 computer
1 connected
1 constant
2 containing
5 controller
1 correct
1 crop
9 data
11 defective
1 designated
3 device
1 disadvantages
1 dram
3 drives
1 ects
1 efficient
1 eliyahou
1 enables
1 enduring
15 erase
6 error
2 every
2 faster
1 few
1 first
2 following
1 full
2 generating
1 harari
1 high
6 improved
1 include
1 incorporate
1 independent
1 initial
2 integrated
1 interfacing
1 inventors
3 large
1 lifetime
4 magnetic
1 make
1 map
4 may
1 memories
1 minimizes
1 moreover
1 moving
1 must

9 cell
14 chips
6 claim
1 combinations
2 comprises
1 conjunction
1 connects
1 consuming
1 contains
2 controlling
6 correction
4 cycles
1 def
2 description
2 detected
4 devices
7 disk
1 drawings
2 during
31 eeprom
1 either
1 embodiments
1 enabling
2 enhanced
6 erased
2 errors
1 exceeds
5 feature
1 fewer
1 fla
30 for
3 further
2 global
1 hard
3 however
2 improvement
4 includes
1 incorporating
1 individually
2 initially
1 intended
4 into
1 involved
3 level
2 limited
1 maintain
1 manner
2 mapping
16 means
33 memory
1 minimizing
1 most
1 much
1 need

> 1 new 1 next 3 non
> 1 nonvolatile 3 not 9 number
> 7 object 2 objects 1 office
> 1 oldest 1 once 11 one
> 3 only 2 operating 12 operation
> 2 operations 2 organized 1 ormed
> 2 other 1 others 1 over
> 1 particular 1 parts 2 patent
> 1 perf 1 perform 1 performance
> 1 performed 1 performing 1 permanent
> 1 place 1 plug 5 plurality
> 1 pointer 1 possible 5 power
> 1 precision 4 predetermined 1 preferred
> 11 present 1 prevented 1 preventing
> 1 printed 1 prior 1 problems
> 3 program 1 programmable 4 programming
> 1 prone 7 provide 2 provided
> 1 put 1 quickly 1 ract
> 1 rather 4 read 2 reading
> 1 ready 1 rectify 1 reduce
> 1 reduced 1 relates 1 relatively
> 1 reliability 1 reliable 1 remaining
> 1 remains 1 remap 2 remapped
> 1 remapping 1 rendered 2 replace
> 3 replaced 1 reprogramming 1 require
> 2 required 1 requirement 1 reset
> 6 responsive 1 retain 1 retarding
> 1 robert 1 room 1 rugged
> 27 said 1 same 1 san
> 1 schemes 13 sector 19 sectors
> 2 select 5 selected 1 selecting
> 1 selection 2 selective 1 semi
> 1 semiconductor 1 serve 1 serves
> 1 should 1 shut 1 signal
> 3 signals 1 significant 1 simultaneously
> 2 solid 1 some 2 soon
> 4 spare 1 specifically 1 sram
> 3 standard 6 state 1 states
> 1 still 1 stopping 16 storage
> 1 stored 4 stress 1 subject
> 5 substitute 1 substitutes 2 substituting
> 3 such 1 suffer 1 summary
> 2 supply 29 system 2 systems
> 1 taken 2 techniques 1 temporary
> 1 term 1 terms 2 than
> 10 that 103 the 3 their
> 1 then 6 thereby 2 therefore
> 2 therein 1 thereon 2 these
> 8 they 6 this 1 those
> 1 throughput 3 time 1 title
> 1 together 1 too 1 trademark
> 1 traditionally 4 typically 1 under
> 1 undergoing 1 understood 1 united
> 1 unnecessary 1 unreliable 1 unsuccessful

> 1 unused	3 use	4 used
> 1 using	4 various	1 virtue
> 4 volatile	3 voltages	1 way
> 1 well	4 when	2 where
> 3 wherein	1 whether	11 which
> 2 while	1 whole	2 will
> 10 with	3 within	1 without
> 12 write	2 writes	1 writing
> 2 written	4 yet	

>---word freq---
>
>---number returned---
>50
>---number returned---
>
>---output options---
>abstracts
>field of search 10
>titles
>---output options---
>

Sales Order Summary:
Customer ID: 681
Sales Transaction Nbr: 57191
Date Posted: August 7, 1997
Product: E003
Quantity: 50

E003 WORD FREQUENCY SEARCH REPORT

Classification Analysis:

1. 365/185.33 Total=19 ORs=3 XRs=16
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 185.01 FLOATING GATE
Sub 185.18 .Particular biasing
Sub 185.29 ..Erase
Sub 185.33 ...Flash

2. 371/10.2 Total=10 ORs=5 XRs=5
Class 371 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
Sub 10.2 REPLACEMENT OF MEMORY SPARE LOCATION, PORTION, OR SEGMENT

3. 365/185.09 Total=9 ORs=2 XRs=7
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 185.01 FLOATING GATE
Sub 185.05 .Particular connection
Sub 185.09 ..Error correction (e.g., redundancy, endurance)

4. 365/185.11 Total=9 ORs=2 XRs=7

Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 185.01 FLOATING GATE
Sub 185.05 .Particular connection
Sub 185.11 ..Bank or block architecture

5. 364/DIG. 1 Total=8 ORs=0 XRs=8
Class 364 ELECTRICAL COMPUTERS AND DATA PROCESSING SYSTEMS
Sub DIG. 1 GENERAL PURPOSE PROGRAMMABLE DIGITAL COMPUTER SYSTEMS

6. 365/200 Total=8 ORs=0 XRs=8
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 189.01 READ/WRITE CIRCUIT
Sub 200 .Bad bit

7. 365/218 Total=8 ORs=4 XRs=4
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 189.01 READ/WRITE CIRCUIT
Sub 218 .Erase

8. 365/201 Total=7 ORs=1 XRs=6
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 189.01 READ/WRITE CIRCUIT
Sub 201 .Testing

9. 395/430 Total=7 ORs=6 XRs=1
Class 395 INFORMATION PROCESSING SYSTEM ORGANIZATION
Sub 427 STORAGE ACCESSING AND CONTROL
Sub 428 .Specific memory composition
Sub 429 ..Solid-state read only memory (ROM)
Sub 430 ...Programmable read only memory (PROM, EEPROM, etc.)

10. 365/185.18 Total=6 ORs=3 XRs=3
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 185.01 FLOATING GATE
Sub 185.18 .Particular biasing

11. 365/185.22 Total=6 ORs=1 XRs=5
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 185.01 FLOATING GATE
Sub 185.18 .Particular biasing
Sub 185.2 ..Reference signal (e.g., dummy cell)
Sub 185.22 ...Verify signal

12. 365/189.09 Total=6 ORs=0 XRs=6
Class 365 STATIC INFORMATION STORAGE AND RETRIEVAL
Sub 189.01 READ/WRITE CIRCUIT
Sub 189.09 .Including reference or bias voltage generator

Patent Report:

Ref Patent Id Issue/File US Class (OR) Title

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1 05535328 Jul 9 1996 395/182.05 Non-volatile memory system card
Feb 23 1995 with flash erasable sectors of
EEprom cells including a mechanism
for substituting defective cells

Inventor: Harari; Eliyahou et al.
Assignee: SanDisk Corporation
Abstract:

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

2 05418752 May 23 1995 365/218 Flash EEPROM system with erase
Oct 20 1992 sector select

Inventor: Harari; Eliyahou et al.
Assignee: Sundisk Corporation
Abstract:

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

3 05297148 Mar 22 1994 371/10.2 Flash eeprom system
Oct 20 1992

Status: certificate of correction has been issued
Inventor: Harari; Eliyahou et al.
Assignee: SunDisk Corporation
Abstract:

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet

another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.,

4 05602987 Feb 11 1997 395/182.06 Flash EEprom system
Dec 29 1993
Inventor: Harari; Eliyahou et al.
Assignee: SanDisk Corporation
Abstract:

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

5 05504760 Apr 2 1996 371/40.1 Mixed data encoding EEPROM system
Nov 8 1993
Inventor: Harari; Eliyahou et al.
Assignee: SanDisk Corporation
Abstract:

In a mixed data encoding scheme for programming data into a flash sector of a flash EEPROM system, a method for determining which data encoding scheme has been used for programming the retrieved data involves examining whether an error correction code of the data indicates an error.

6 05200959 Apr 6 1993 371/21.6 Device and method for defect
Oct 17 1989 handling in semi-conductor memory
Inventor: Gross; Stephen et al.
Assignee: SunDisk Corporation
Abstract:

A solid-state memory array such as an electrically erasable programmable read only memory (EEprom) or Flash EEprom array is used to store sequential data in a prescribed order. The memory includes a first information list containing addresses and defect types of previously detected defects. The defects are listed in the same prescribed order as that of the data. Only a simple controller is required to reference the information list so that writing or reading of the data will skip over the defective locations in the memory. New defects may be detected during writing by failure in verification, and those new defects will also be skipped. The memory also includes a second information list maintained by the controller. As data is written to the memory, addresses of file-markers and defects detected by write failure are entered into the list in the same prescribed order. This second list is referenced with the first list by the controller in subsequent reading to skip over both the previously and the newly detected defects.

7 05396468 Mar 7 1995 365/218 Streamlined write operation for

Nov 8 1993 EEPROM system
Inventor: Harari; Eliyahou et al.
Assignee: SunDisk Corporation
Abstract:
Various optimizing techniques are used for erasing semiconductor electrically erasable programmable read only memories (EEPROM). An erase algorithm accomplishes erasing of a group of memory cells by application of incremental erase pulses. Techniques include a 2-phase verification process interleaving between pulse applications; special handling of a sample of cells within each erasable unit group; defects handling; and adaptive initial erasing voltages. A streamlined write operation on a flash sector of the EEPROM is implemented by employing the optimized erase in an efficient manner. The write operation includes an initial quick erase of the sector followed by programming of data and verification. Only on those infrequent occasions when a failure occurs as manifested during program verification that the optimized erase will need be evoked.

8 05438573 Aug 1 1995 371/10.3 Flash EEPROM array data and header
Jun 1 1994 file structure
Inventor: Mangan; John S. et al.
Assignee: SunDisk Corporation et al.
Abstract:
A file structure employed in a flash electrically erasable and programmable read only memory ("EEPROM") system and aspects of forming and using certain data fields within such a file structure. An array of rows and columns of EEPROM memory cells is divided into blocks of cells that are separately addressable for the purpose of erasing an entire block of cells at the same time. Each block contains several rows of cells with certain columns thereof storing a sector of data, typically 512 bytes of data, and other columns of cells within the same rows being used as spare cells to replace any defective sector data cells and store overhead (header) information about the block and the data sector. Such overhead information includes pointers to locations of any defective sector data cells within the block, whether the block has been mapped out in favor of another block, error correction codes for the sector data and the header information, and other similar types of information.

9 05471478 Nov 28 1995 371/10.3 Flash EEPROM array data and header
Mar 10 1995 file structure
Inventor: Mangan; John S. et al.
Assignee: SunDisk Corporation et al.
Abstract:
A file structure employed in a flash electrically erasable and programmable read only memory ("EEPROM") system and aspects of forming and using certain data fields within such a file structure. An array of rows and columns of EEPROM memory cells is divided into blocks of cells that are separately addressable for the purpose of erasing an entire block of cells at the same time. Each block contains several rows of cells with certain columns thereof storing a sector of data, typically 512 bytes of data, and other columns of cells within the same rows being used as spare cells to replace any defective sector data cells and store overhead (header) information about the block and the data sector. Such overhead information includes pointers to locations of any defective sector data cells within the block, whether the block has been mapped out in favor of

another block, error correction codes for the sector data and the header information, and other similar types of information.

10 05270979 Dec 14 1993 365/185.09 Method for optimum erasing of
Mar 15 1991 EEPROM
Inventor: Harari; Eliyahou et al.
Assignee: SunDisk Corporation
Abstract:
Various optimizing techniques are used for erasing semiconductor electrically erasable programmable read only memories (EEPROM). An erase algorithm accomplishes erasing of a group of memory cells by application of incremental erase pulses. Techniques include a 2-phase verification process interleaving between pulse applications; special handling of a sample of cells within each erasable unit group; defects handling; adaptive initial erasing voltages; and single-and hybrid-phase algorithms with sector to sector estimation of erase characteristics by table lookup. Techniques are also employed for controlling the uniformity of program/erase cycling of cells in each erasable unit group. Defects handling includes an adaptive data encoding scheme.

11 05369615 Nov 29 1994 365/185.19 Method for optimum erasing of
Nov 8 1993 EEPROM
Status: certificate of correction has been issued
Inventor: Harari; Eliyahou et al.
Assignee: SunDisk Corporation
Abstract:
Various optimizing techniques are used for erasing semiconductor electrically erasable programmable read only memories (EEPROM), An erase algorithm accomplishes erasing of a group of memory cells by application of incremental erase pulses, Techniques include a 2-phase verification process interleaving between pulse applications; special handling of a sample of cells within each erasable unit group; defects handling; adaptive initial erasing voltages; and single- and hybrid-phase algorithms with sector to sector estimation of erase characteristics by table lookup. Techniques are also employed for controlling the uniformity of program/erase cycling of cells in each erasable unit group, Defects handling includes an adaptive data encoding scheme.

12 05568424 Oct 22 1996 365/185.33 Programmable power generation
Jun 7 1995 circuit for flash EEPROM memory systems
Inventor: Cernea; Raul-Adrian et al.
Assignee: SanDisk Corporation
Abstract:
An flash EEPROM system functioning as a mass storage medium for a host computer includes a controller and at least one flash EEPROM memory module. The flash EEPROM memory module includes at least one flash EEPROM chip having an on-chip programmable power generation circuit including a high voltage generator circuit capable of generating a high voltage Vpp from a logic level voltage Vdd provided to the chip, a serial protocol logic circuit, a data latch, a data bus, a register address decoder, and a multi-voltage generator/regulator. The multi-voltage generator/regulator includes a plurality of registers and provides the programming, reading, and erasing voltages required for proper operation of the flash EEPROM

system from digital values stored in the plurality of registers by the controller. The high voltage generator circuit includes both high current and low current charge pump circuits for generating the high voltage Vpp. The high current charge pump circuit is connected to relatively large off-chip charge storage devices, and the low current charge pump circuit is connected to relatively small on-chip charge storage devices. The controller may activate one or the other of the high or low current charge pump circuits through control signals connected to enabling circuitry respectively connected to the high and low current charge pump circuits. Alternatively, the controller may deactivate both the high and low current charge pump circuits and cause the high voltage Vpp to be provided from other circuitry on another flash EEPROM chip in the flash EEPROM module.

13 05592420 Jan 7 1997 365/185.18 Programmable power generation
Jun 7 1995 circuit for flash EEPROM memory systems

Inventor: Cernea; Raul-Adrian et al.
Assignee: SanDisk Corporation
Abstract:

An flash EEPROM system functioning as a mass storage medium for a host computer includes a controller and at least one flash EEPROM memory module. The flash EEPROM memory module includes at least one flash EEPROM chip having an on-chip programmable power generation circuit including a high voltage generator circuit capable of generating a high voltage Vpp from a logic level voltage Vdd provided to the chip, a serial protocol logic circuit, a data latch, a data bus, a register address decoder, and a multi-voltage generator/regulator. The multi-voltage generator/regulator includes a plurality of registers and provides the programming, reading, and erasing voltages required for proper operation of the flash EEPROM system from digital values stored in the plurality of registers by the controller. The high voltage generator circuit includes both high current and low current charge pump circuits for generating the high voltage Vpp. The high current charge pump circuit is connected to relatively large off-chip charge storage devices, and the low current charge pump circuit is connected to relatively small on-chip charge storage devices. The controller may activate one or the other of the high or low current charge pump circuits through control signals connected to enabling circuitry respectively connected to the high and low current charge pump circuits. Alternatively, the controller may deactivate both the high and low current charge pump circuits and cause the high voltage Vpp to be provided from other circuitry on another flash EEPROM chip in the flash EEPROM module.

14 05621685 Apr 15 1997 365/185.18 Programmable power generation
Jun 7 1995 circuit for flash EEPROM memory systems

Inventor: Cernea; Raul-Adrian et al.
Assignee: SanDisk Corporation
Abstract:

An flash EEPROM system functioning as a mass storage medium for a host computer includes a controller and at least one flash EEPROM memory module. The flash EEPROM memory module includes at least one flash EEPROM chip having an on-chip programmable power generation circuit including a high voltage generator circuit capable of generating a high voltage Vpp from a logic level voltage Vdd provided to the chip, a serial protocol

logic circuit, a data latch, a data bus, a register address decoder, and a multi-voltage generator/regulator. The multi-voltage generator/regulator includes a plurality of registers and provides the programming, reading, and erasing voltages required for proper operation of the flash EEPROM system from digital values stored in the plurality of registers by the controller. The high voltage generator circuit includes both high current and low current charge pump circuits for generating the high voltage Vpp. The high current charge pump circuit is connected to relatively large off-chip charge storage devices, and the low current charge pump circuit is connected to relatively small on-chip charge storage devices. The controller may activate one or the other of the high or low current charge pump circuits through control signals connected to enabling circuitry respectively connected to the high and low current charge pump circuits. Alternatively, the controller may deactivate both the high and low current charge pump circuits and cause the high voltage Vpp to be provided from other circuitry on another flash EEPROM chip in the flash EEPROM module.

15 05508971 Apr 16 1996 365/185.23 Programmable power generation
Oct 17 1994 circuit for flash EEPROM memory systems

Inventor: Cernea; Raul-Adrian et al.
Assignee: SanDisk Corporation
Abstract:

An flash EEPROM system functioning as a mass storage medium for a host computer includes a controller and at least one flash EEPROM memory module. The flash EEPROM memory module includes at least one flash EEPROM chip having an on-chip programmable power generation circuit including a high voltage generator circuit capable of generating a high voltage Vpp from a logic level voltage Vdd provided to the chip, a serial protocol logic circuit, a data latch, a data bus, a register address decoder, and a multi-voltage generator/regulator. The multi-voltage generator/regulator includes a plurality of registers and provides the programming, reading, and erasing voltages required for proper operation of the flash EEPROM system from digital values stored in the plurality of registers by the controller. The high voltage generator circuit includes both high current and low current charge pump circuits for generating the high voltage Vpp. The high current charge pump circuit is connected to relatively large off-chip charge storage devices, and the low current charge pump circuit is connected to relatively small on-chip charge storage devices. The controller may activate one or the other of the high or low current charge pump circuits through control signals connected to enabling circuitry respectively connected to the high and low current charge pump circuits. Alternatively, the controller may deactivate both the high and low current charge pump circuits and cause the high voltage Vpp to be provided from other circuitry on another flash EEPROM chip in the flash EEPROM module.

16 05563825 Oct 8 1996 365/185.18 Programmable power generation
Jun 7 1995 circuit for flash eeprom memory systems

Inventor: Cernea; Raul-Adrian et al.
Assignee: SanDisk Corporation
Abstract:

An flash EEPROM system functioning as a mass storage medium for a host computer includes a controller and at least one flash EEPROM memory

module. The flash EEPROM memory module includes at least one flash EEPROM chip having an on-chip programmable power generation circuit including a high voltage generator circuit capable of generating a high voltage Vpp from a logic level voltage Vdd provided to the chip, a serial protocol logic circuit, a data latch, a data bus, a register address decoder, and a multi-voltage generator/regulator. The multi-voltage generator/regulator includes a plurality of registers and provides the programming, reading, and erasing voltages required for proper operation of the flash EEPROM system from digital values stored in the plurality of registers by the controller. The high voltage generator circuit includes both high current and low current charge pump circuits for generating the high voltage Vpp. The high current charge pump circuit is connected to relatively large off-chip charge storage devices, and the low current charge pump circuit is connected to relatively small on-chip charge storage devices. The controller may activate one or the other of the high or low current charge pump circuits through control signals connected to enabling circuitry respectively connected to the high and low current charge pump circuits. Alternatively, the controller may deactivate both the high and low current charge pump circuits and cause the high voltage Vpp to be provided from other circuitry on another flash EEPROM chip in the flash EEPROM module.

17 05163021 Nov 10 1992 365/185.03 Multi-state EEprom read and write
Jul 22 1991 circuits and techniques
Inventor: Mehrotra; Sanjay et al.
Assignee: SunDisk Corporation
Abstract:

Improvements in the circuits and techniques for read, write and erase of EEprom memory enable nonvolatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells which closely track and make adjustment for the variations presented by the memory cells. In one embodiment, each Flash sector of memory cells has its own reference cells for reading the cells in the sector, and a set of reference cells also exists for the whole memory chip acting as a master reference. In another embodiment, the reading is made relative to a set of threshold levels simultaneously by means of a one-to-many current mirror circuit. In improved write or erase circuits, verification of the written or erased data is done in parallel on a group of memory cells at a time and a circuit selectively inhibits further write or erase to those cells which have been correctly verified. Other improvements includes programming the ground state after erase, independent and variable power supply for the control gate of EEprom memory cells.

18 05428621 Jun 27 1995 371/21.4 Latent defect handling in EEPROM
Sep 21 1992 devices
Status: certificate of correction has been issued
Inventor: Mehrotra; Sanjay et al.
Assignee: SunDisk Corporation
Abstract:

A memory system having a two dimensional array of EEPROM or Flash EEPROM cells is addressable by rows and columns. A word line is connected to the control gates of all the cells in each row, an erase line is

connected to all the erase gates of each sector of cells, and a pair of bit lines are connected respectively to all the sources and drains of each column of cells. The memory system incorporates a word line current detector and an erase line current detector in addition to the usual bit line current detectors. The leakage current of each of the lines are measured after predetermined memory events such as program or erase operations. When a defective row or column is detected, it is electrically isolated from other columns by programming and is mapped out and replaced. Data recovery schemes include reading a defective column by a switched-memory-source-drain technique.

19 05172338 Dec 15 1992 365/185.03 Multi-state EEprom read and write
Apr 11 1990 circuits and techniques
Status: certificate of correction has been issued
Inventor: Mehrotra; Sanjay et al.
Assignee: Sundisk Corporation
Abstract:

Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells which closely track and make adjustment for the variations presented by the memory cells. In one embodiment, each Flash sector of memory cells has its own reference cells for reading the cells in the sector, and a set of reference cells also exists for the whole memory chip acting as a master reference. In another embodiment, the reading is made relative to a set of threshold levels simultaneously by means of a one-to-many current mirror circuit. In improved write or erase circuits, verification of the written or erased data is done in parallel on a group of memory cells at a time and a circuit selectively inhibits further write or erase to those cells which have been correctly verified. Other improvements includes programming the ground state after erase, independent and variable power supply for the control gate of EEprom memory cells.

20 05532962 Jul 2 1996 365/201 Soft errors handling in EEPROM
Mar 21 1995 devices
Inventor: Auclair; Daniel L. et al.
Assignee: SanDisk Corporation
Abstract:

Soft errors occur during normal use of a solid-state memory such as EEPROM or Flash EEPROM. A soft error results from the programmed threshold voltage of a memory cell being drifted from its originally intended level. The error is initially not readily detected during normal read until the cumulative drift becomes so severe that it develops into a hard error. Data could be lost if enough of these hard errors swamps available error correction codes in the memory. A memory device and techniques therefor are capable of detecting these drifts and substantially maintaining the threshold voltage of each memory cell to its intended level throughout the use of the memory device, thereby resisting the development of soft errors into hard errors.

21 05517453 May 14 1996 365/185.12 Memory with multiple erase modes

Sep 15 1994
Inventor: Strain; Robert J. et al.
Assignee: National Semiconductor Corporation
Abstract:

An electrically-erasable, electrically programmable read-only memory (EEPROM) with multiple erase modes identifies sections of memory cells that have not received a write operation subsequent to the most recent erase operation and inhibits erasure of the memory cells in such sections. An indicator column is formed from indicator memory cells added to each section. During a write operation in which a section is first erased and then programmed, the EEPROM reads the indicator memory cell added to the section and inhibits the erase of the section if the memory cells in the section are in an erased state.

22 05337275 Aug 9 1994 365/189.01 Method for releasing space in
Nov 1 1993 flash EEPROM memory array to allow the storage of compressed data

Inventor: Garner; Richard P.
Assignee: Intel Corporation
Abstract:

A process for releasing sectors of a flash EEPROM memory array in which data furnished by a host computer is stored in compressed form so that memory space used for the sectors may be used to store new data. The flash EEPROM memory array includes a plurality of individually erasable blocks and stores sectors of data in such blocks with a header providing a logical sector number, an indication of validity of data stored. The process stores a list of files and sectors which have been deleted by a host computer in a first table in host memory, stores a value indicating an amount of free space remaining in the flash EEPROM memory array, provides a first signal to the host computer when the value indicating the amount of free space falls below a first predetermined value to indicate that sectors listed in the first table should be released, and provides a second signal when the value indicating the amount of free space falls below a second predetermined value to terminate writes to and erasures of the array.

23 05603001 Feb 11 1997 395/430 Semiconductor disk system having a
May 5 1995 plurality of flash memories

Inventor: Sukegawa; Hiroshi et al.
Assignee: Kabushiki Kaisha Toshiba
Abstract:

A NAND bus interface independently receives 16 ready/busy signals from 16 flash EEPROM chips and thereby separately manages the operating states of these flash EEPROMs. Once a flash EEPROM as a write access target is set in a ready state, a write access to this write access target flash EEPROM is started without waiting for completion of the operations of all the flash EEPROMs. Each flash EEPROM is of a command control type capable of automatically executing a write operation. This allows parallel processing of the flash EEPROMs, i.e., a write access to a given EEPROM can be performed while a data write to another flash EEPROM is being executed. An ECC calculating circuit calculates a data string transferred in units of 256 bytes from a data buffer by a processor, and generates an ECC corresponding to that data string. The 256-byte data string is added with the generated ECC and transferred to a data register of a flash

EEPROM. Even if abnormal cells are produced at the same bit position in a plurality of pages of a flash EEPROM, only one abnormal cell is contained in a data string as an object of the ECC calculation. This makes it possible to perform error detection and correction by a common simple ECC calculation without using any complicated ECC arithmetic expression with a high data recovery capability.

24 05530673 Jun 25 1996 365/185.09 Flash memory control method and
Apr 8 1994 information processing system
therewith

Inventor: Tobita; Tsunehiro et al.
Assignee: Hitachi, Ltd. et al.
Abstract:

A control method and system when a flash memory is used as a semiconductor disk or a main memory in an information processing system. A semiconductor file system comprises a first nonvolatile memory electrically erasable, a second nonvolatile memory not electrically erasable, a volatile memory, a controller which controls the memories, and a control section which controls the controller wherein a physical address corresponding to a logical address specified from an external system is accessed. The first nonvolatile memory stores data for the external system to perform operations, first management information indicating the correspondence between physical addresses at which the data is stored and logical addresses, and second management information indicating a state of the first nonvolatile memory. The second nonvolatile memory previously stores interface information required for inputting and outputting the data from and to the external system and read-only data of the data. The controller comprises control means for determining a physical sector address forming predetermined high-order bits of the physical address when data is output from the first nonvolatile memory or when data is input to the volatile memory, means for storing the determined physical sector address, and means for consecutively generating addresses in a sector determined by the physical sector address.

25 05581723 Dec 3 1996 395/430 Method and apparatus for retaining
Feb 19 1993 flash block structure data during
erase operations in a flash EEPROM
memory array

Inventor: Hasbun; Robert N. et al.
Assignee: Intel Corporation
Abstract:

A method for reliably storing management data in a flash EEPROM memory array, which array is divided into a plurality of individually-erasable blocks of memory cells and in which each of the blocks of memory cells has stored thereon data regarding management of the array during a cleanup process in which valid data stored in a first block is written to another block of the array, and then the first block is erased. The process includes the steps of storing data regarding management of the array from the first block in random access memory and, in an enhanced process, on another block before erasure of the first block. The data may then be rewritten to the first block after the erase. With the enhanced process, a special identification is provided to the data regarding the management of the array stored on another block which is outside the normal identification range for the host computer so that the specially

identified data is not lost during a power loss during an erase process and may be detected after power is restored to the system.

26 05357475 Oct 18 1994 395/430 Method for detaching sectors in a
Oct 30 1992 flash EEPROM memory array
Inventor: Hasbun; Robert N. et al.
Assignee: Intel Corporation
Abstract:

A process for releasing sectors of a flash EEPROM memory array which includes a plurality of individually erasable blocks and stores sectors of data in such blocks with a header providing a logical sector number, an indication of validity of data stored, and an indication of whether data is stored with the header. The process includes the steps of finding the header of a sector with data to be released, setting the indication of validity of the data stored to indicate that the data is invalid, and writing a new header for the sector to a new position in the array without data and with an indication that data is not attached.

27 05341339 Aug 23 1994 365/185.11 Method for wear leveling in a
Nov 1 1993 flash EEPROM memory
Inventor: Wells; Steven E.
Assignee: Intel Corporation
Abstract:

In a process for cleaning up a flash EEPROM memory array separated into blocks which may be separately erased, in which process all valid data is first written to other blocks of the array, and then the block is erased, the improvement including the step of determining a block to clean up based on a comparison of the number of invalid sectors each block includes and the number of switching operations which each block has undergone.

28 05546402 Aug 13 1996 371/10.2 Flash-erase-type nonvolatile
Jun 7 1995 semiconductor storage device
Inventor: Niijima; Hideto et al.
Assignee: International Business Machines Corporation
Abstract:

An array of memory cells is physically divided into a data area and a tag area so that respective parts of the two areas share a word line but can be separately erased en bloc. The data area and tag area sharing one word line constitute a single logical unit. In the logical unit, the tag area stores location information for defective memory cells in the corresponding data area. On the basis of this information, the system avoids the use of the defective memory cells. The defective memory cell information is programmed in a test step performed after chip manufacture and, at the same time, ECCs are generated for the defective memory cell information and written to the tag area. Furthermore, the system is informed of the invalidity of the data area that shares a word line with a tag area by writing predetermined data to the tag area. Even when the data area is erased en bloc, the tag area is not erased and the defective memory cell information is retained there.

29 05509018 Apr 16 1996 371/10.2 Flash-erase-type nonvolatile
Sep 10 1993 semiconductor storage device
Inventor: Niijima; Hideto et al.

Assignee: International Business Machines Corporation
Abstract:

An array of memory cells is physically divided into a data area and a tag area so that respective parts of the two areas share a word line but can be separately erased en bloc. The data area and tag area sharing one word line constitute a single logical unit. In the logical unit, the tag area stores location information for defective memory cells in the corresponding data area. On the basis of this information, the system avoids the use of the defective memory cells. The defective memory cell information is programmed in a test step performed after chip manufacture and, at the same time, ECCs are generated for the defective memory cell information and written to the tag area. Furthermore, the system is informed of the validity of the data area that shares a word line with a tag area by writing predetermined data to the tag area. Even when the data area is erased en bloc, the tag area is not erased and the defective memory cell information is retained there.

30 05553261 Sep 3 1996 395/430 Method of performing clean-up of a
Apr 1 1994 solid state disk while executing a
read command

Inventor: Hasbun; Robert N. et al.
Assignee: Intel Corporation
Abstract:

A method of executing states of a clean-up state machine while executing a command from a host CPU to read a sector of data stored within a memory array. First, a number of sectors of data are copied from the memory array into a sector buffer. Then, while the host CPU is reading sectors from the sector buffer, a number of states of a clean-up state machine are executed to aid in the conversion of invalid user data into free memory. Also described is a solid state memory disk that converts invalid sectors of data to free memory while executing a read command from a host CPU.

31 05379401 Jan 3 1995 395/430 Flash memory card including
Feb 16 1994 circuitry for selectively
providing masked and unmasked
ready/busy output signals

Inventor: Robinson; Kurt B. et al.
Assignee: Intel Corporation
Abstract:

A flash memory card is described which includes a first flash memory and a second flash memory. The first flash memory includes an unmasked first output that enters a first state if the first flash memory is ready and a second state if the first flash memory is busy. The second flash memory includes an unmasked second output that enters the first state if the second flash memory is ready and the second state if the second flash memory is busy. The flash memory card also includes a circuit for selectively providing one of (1) a masked first output (2) the unmasked first output, (3) a masked second output, and (4) the unmasked second output. A latch provides a first ready output signal for the flash memory card. The first ready output signal indicates a first transition from the second state to the first state by one of the unmasked first output of the first flash memory and the unmasked second output of the second flash memory. A circuit is also provided for clearing the first ready output

signal from the latch.

32 05388248 Feb 7 1995 365/52 Flash memory card including plural
Feb 16 1994 flash memories and circuitry for selectively outputting ready/busy signals in different operating modes

Status: certificate of correction has been issued
Inventor: Robinson; Kurt B. et al.
Assignee: Intel Corporation
Abstract:

A flash memory card is described which has a plurality of flash memories, each having a ready/busy output for indicating whether its respective one of the plurality of flash memories is busy or ready. A register circuit is provided for storing a plurality of mask data. A mode circuit is provided for choosing one of a first mode and a second mode, wherein a first mode signal is produced if the first mode is chosen and a second mode signal is produced if the second mode is chosen. A logic circuit is provided for performing logical operations with respect to the ready/busy output for each of the plurality of flash memories and the mask data in accordance with whether the first mode signal or the second mode signal is produced. If the first mode is chosen, the logic circuit produces a ready signal output for the flash memory card only if the ready/busy output of all the plurality of flash memories is ready. If the second mode is chosen, the logic circuit produces a ready signal output for the flash memory card each time any flash memory goes from being busy to being ready.

33 05452311 Sep 19 1995 371/51.1 Method and apparatus to improve
Oct 30 1992 read reliability in semiconductor memories

Inventor: Wells; Steven et al.
Assignee: Intel Corporation
Abstract:

Apparatus for controlling a length of a period during which the output circuitry of a memory array waits before latching the output data including apparatus for detecting the presence of an error in data read from an memory array, apparatus for providing a first value to determine a wait period, apparatus responsive to the detection of an error for providing a second value, apparatus responsive to the first value for generating a signal to latch a data output from the memory array after a first period and responsive to the second value for generating a signal to latch a data output from the memory array after a second period.

34 05566194 Oct 15 1996 371/51.1 Method and apparatus to improve
Jun 6 1995 read reliability in semiconductor memories

Inventor: Wells; Steven et al.
Assignee: Intel Corporation
Abstract:

Apparatus for controlling a length of a period during which the output circuitry of a memory array waits before latching the output data including apparatus for detecting the presence of an error in data read from an memory array, apparatus for providing a first value to determine a

wait period, apparatus responsive to the detection of an error for providing a second value, apparatus responsive to the first value for generating a signal to latch a data output from the memory array after a first period and responsive to the second value for generating a signal to latch a data output from the memory array after a second period.

35 05490264 Feb 6 1996 395/481 Generally-diagonal mapping of
Sep 30 1993 address space for row/column organizer memories

Inventor: Wells; Steven et al.
Assignee: Intel Corporation
Abstract:

A method for storing data in a generally-diagonal pattern in blocks of a flash EEPROM array by which the least number of memory cells are affected by a failure of either a row conductor or a column conductor, and apparatus for addressing the flash array to produce such a generally-diagonal storage pattern. The arrangement allows the simplest forms of error detection and correction circuitry to be utilized.

36 05473753 Dec 5 1995 395/182.03 Method of managing defects in
Oct 30 1992 flash disk memories

Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:

A method for monitoring the operations of a flash memory array divided into individually erasable blocks of memory in order to assure the integrity of data stored in the array in which each read or write operation is verified to detect an error which may have occurred in the operation including the steps of attempting at least one retry operation whenever an error occurs to determine whether the error is repeatable, marking the block to indicate valid data should be removed from the block if the error is found to be repeatable, removing the valid information from the block if the error is found to be repeatable, and removing a block with a repeatable error from operation.

37 05577194 Nov 19 1996 395/182.06 Method of managing defects in
Aug 7 1995 flash disk memories

Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:

A method for monitoring the operations of a flash memory array divided into individually erasable blocks of memory in order to assure the integrity of data stored in the array in which each read or write operation is verified to detect an error which may have occurred in the operation including the steps of attempting at least one retry operation whenever an error occurs to determine whether the error is repeatable, marking the block to indicate valid data should be removed from the block if the error is found to be repeatable, removing the valid information from the block if the error is found to be repeatable, and removing a block with a repeatable error from operation.

38 05369616 Nov 29 1994 365/185.22 Method for assuring that an erase
Mar 7 1994 process for a memory array has been properly completed

Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:

A method for insuring that an erase operation practiced on a block of flash EEPROM transistors is carried out reliably including the steps of: writing whenever the erasure of a block of the flash EEPROM array is to commence to a position in the array to indicate that an erasure of the block has commenced, writing whenever the erasure of a block of the flash EEPROM array is complete to the position in the array to indicate that an erasure of the block has been completed, testing to determine any positions in the array which indicate that an erasure of a block has commenced but not been completed upon applying power to the flash EEPROM array, and reinitiating an erase if any positions in the array exist which indicate that an erasure of a block has commenced but not been completed.

39 05544119 Aug 6 1996 365/185.11 Method for assuring that an erase
Sep 6 1995 process for a memory array has been properly completed

Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:

A method for insuring that an erase operation practiced on a block of flash EEPROM transistors is carried out reliably including the steps of: writing whenever the erasure of a block of the flash EEPROM array is to commence to a position in the array to indicate that an erasure of the block has commenced, writing whenever the erasure of a block of the flash EEPROM array is complete to the position in the array to indicate that an erasure of the block has been completed, testing to determine any positions in the array which indicate that an erasure of a block has commenced but not been completed upon applying power to the flash EEPROM array, and reinitiating an erase if any positions in the array exist which indicate that an erasure of a block has commenced but not been completed.

40 05375222 Dec 20 1994 395/430 Flash memory card with a
Mar 31 1992 ready/busy mask register

Status: certificate of correction has been issued
Inventor: Robinson; Kurt B. et al.
Assignee: Intel Corporation
Abstract:

A flash memory card is described which has a ready/busy mask register. First and second flash memories of the flash memory card have respective first and second outputs indicating ready or busy status for the first and second memories. The ready/busy mask register contains mask data. Logic circuitry performs (1) a first logical operation between a first output and a first mask datum to produce a first masked output, (2) a second logical operation between a second output and a second mask datum to produce a second masked output, and (3) a third logical operation between the first masked output and the second masked output to produce a flash memory card ready/busy output. The flash memory card has circuitry for providing a ready output signal that indicates a first (in time) transition from a busy mode to a ready mode by either the first flash memory or the second flash memory of the flash memory card.

41 05541886 Jul 30 1996 365/230.01 Method and apparatus for storing

Dec 27 1994 control information in multi-bit non-volatile memory arrays

Inventor: Hasbun; Robert
Assignee: Intel Corporation
Abstract:

A memory array circuit including a plurality of non-volatile memory cells adapted to selectively store data in either single bit mode or a multi-bit mode, control circuitry for causing control information data to be stored in first preselected ones of the plurality of cells and other data to be stored in other preselected ones of the plurality of cells, and circuitry for accessing the plurality of cells to read, program and erase the cells, the accessing circuitry functioning to access cells for storing control information data in single bit mode and cells for storing other data in either single bit or multi-bit mode.

42 05455800 Oct 3 1995 365/218 Apparatus and a method for
Oct 27 1994 improving the program and erase performance of a flash EEPROM memory array

Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:

A voltage Vpp is provided for use in programing and erasing transistors which transistors normally switch with a voltage Vpp centering at X volts in a range varying from X plus Y to X minus Y volts. When transistors in an array are selected to operate in this range, a significant number of the blocks of memory transistors require as much as three times as long to program and erase as do typical memory transistors. The invention provides circuitry for furnishing a voltage Vpp to program and erase the blocks of the memory array which voltage is controlled to be in a range of X to X+Y volts and centers around X+ Y volts.

43 05459850 Oct 17 1995 395/497.02 Flash solid state drive that
Feb 19 1993 emulates a disk drive and stores variable length and fixed lenth data blocks

Status: certificate of correction has been issued
Inventor: Clay; Donald W. et al.
Assignee: Conner Peripherals, Inc.
Abstract:

A flash solid state drive, having a flash solid state memory compatible with ATA/IDE Interface standards to be connected to a host for storing or retrieving sectors of data, where each sector contains 512 bytes of data, each sector is addressed by a cylinder, head and sector number CHS. The host provides, for a read or write operation, the number of sectors to be stored or retrieved, the CHS for each sector to be stored or retrieved and the data for the sectors to be stored. The solid state memory has stored therein a header for each CHS address that can be issued by the host, the header having indicia identifying the data block and indicating where the data for the data block is stored in the solid state memory. The flash solid state device comprises a translator means for translating the CHS address into a logic sector number LSN for identifying sectors in the flash solid state drive and a controller for converting sectors received from the host into variable length sectors to be stored

in the flash solid state memory.

44 05199033 Mar 30 1993 395/182.05 Solid state memory array using
May 10 1990 address block bit substitution to compensate for non-functional storage cells

Inventor: McGeoch; Bruce M. et al.
Assignee: Quantum Corporation
Abstract:

A solid state memory array includes an address bus and a bidirectional data bus and a plurality of partly defective VLSI memory array chips each containing at least one megabit of data storage capacity, having defective memory cell locations, being connected to the address bus, and providing plural data storage bit positions. Each memory array chip has a bidirectional tri-state driver connected between the bit lines thereof and corresponding ones of the data bus. At least one VLSI substitution memory chip contains at least one megabyte of data storage capacity, is connected to the address bus and provides plural data storage bit positions. A substitution chip tri-state driver is connected between the bit lines of the substitution memory chip and all of the parallel data bit lines of the data bus. A programmable read only memory is connected to be addressed by the address bus and is programmed for putting out a binary coded value which has been coded to identify each said defective memory cell location of each one of the memory array chips. A decoder is connected to receive and decode the binary coded value into tri-state driver control values and applies the values to the substitution chip tri-state driver and to one of the memory array chip bidirectional tri-state drivers so as to disable the memory array chip associated with the particular chip driver when a defective memory cell location thereof is addressed, and to enable the substitution memory chip at the particular location and connect it to the data bus in place of the associated memory array chip.

45 05544118 Aug 6 1996 365/218 Flash EEPROM system cell array
Mar 7 1995 with defect management including an error correction scheme

Inventor: Harari; Eliyahou
Abstract:

A memory system made up of electrically programmable read only memory (EPROM) or flash electrically erasable and programmable read only memory (EEPROM) cells. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. More than one bit is stored in a cell by establishing more than two distinct threshold states into which the cell is programmed. A series of pulses of increasing voltage is applied to each addressed memory cell during its programming, the state of the cell being read in between pulses. The pulses are terminated upon the addressed cell reaching its desired state or a preset maximum number of pulses has been reached. An intelligent erase algorithm prolongs the useful life of the memory cells. A series of pulses is also applied to a block of cells being erased, the state of at least a sample number of cells being read in between pulses. The erasing process is stopped when the cells being read are determined to have reached a fully erased state or one of a number of other conditions has occured. Individual records of the number of erase cycles experienced by blocks of flash EEPROM cells are kept, preferably as part of the blocks themselves,

in order to maintain an endurance history of cells within the block. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.

46 05224070 Jun 29 1993 365/185.33 Apparatus for determining the
Dec 11 1991 conditions of programming
circuitry used with flash EEPROM
memory
Status: certificate of correction has been issued
Inventor: Fandrich; Mickey L. et al.
Assignee: Intel Corporation
Abstract:
A circuit which monitors the internal state of flash memory array programming circuitry and conveys that state to circuitry external to the flash memory array so that external circuitry need not delay during any period in which a programming operation is taking place within the flash memory array.

47 05341330 Aug 23 1994 365/185.33 Method for writing to a flash
Nov 1 1993 memory array during erase suspend
intervals
Inventor: Wells; Steven E. et al.
Assignee: Intel Corporation
Abstract:
A method for writing data to an entry in a portion of a flash EEPROM memory array during a period in which that portion of the array is being erased and writing is prohibited. The method includes writing the data to a new entry position apart from the portion of the array which is being erased along with a revision number which is greater than the revision number of the original data in the original portion of the array, writing of the busy condition of the original entry to a temporary storage position apart from the portion of the array which is being erased, and invalidating entries listed in the temporary storage position when the erase operation is concluded.

48 05422855 Jun 6 1995 365/226 Flash memory card with all zones
Sep 30 1994 chip enable circuitry
Inventor: Eslick; Russell D. et al.
Assignee: Intel Corporation
Abstract:
A flash memory card is described. One flash memory card has addressable circuitry for selectively causing first, second, and third flash memories to operate in an active mode concurrently.

49 05153880 Oct 6 1992 371/10.2 Field-programmable redundancy
Mar 12 1990 apparatus for memory arrays
Inventor: Owen; William H. et al.
Assignee: Xicor, Inc.
Abstract:
A field-programmable redundancy apparatus for integrated circuit semiconductor memory arrays is disclosed. The present invention allows the user to replace a defective memory cell with a redundant memory cell while the integrated circuit memory array is in the field. The user communicates

with the redundancy apparatus over the standard signal paths with standard voltage levels of the integrated circuit semiconductor memory array. The redundancy apparatus detects a predetermined code sequence on one or more of the address and data lines of the memory array to enter a special redundancy-reconfiguration mode. In the reconfiguration mode, the redundancy apparatus provides information on the availability and functionality of the redundant memory cells and enables the user to replace a defective memory cell with a selected redundant memory cell. The field-programmable redundance apparatus may comprise nonvolatile memory means, such as EEPROM's, to store the replacements of primary memory cells with redundant memory cells. In the reconfiguration mode, detection of a second predetermined code sequence causes the reconfiguration mode to be exited.

50 05161157 Nov 3 1992 371/10.2 Field-programmable redundancy
Nov 27 1991 apparatus for memory arrays
Status: certificate of correction has been issued
Inventor: Owen; William H. et al.
Assignee: Xicor, Inc.
Abstract:

A field-programmable redundancy apparatus for integrated circuit semiconductor memory arrays is disclosed. The present invention allows the user to replace a defective memory cell with a redundant memory cell while the integrated circuit memory array is in the field. The user communicates with the redundancy apparatus over standard signal paths of the integrated circuit semiconductor memory array and with standard voltage levels. The redundancy apparatus detects a predetermined code sequence on one or more of the address and data lines of the memory array to enter a special redundancy-reconfiguration mode. In the reconfiguration mode, the redundancy apparatus provides information on the availability and functionality of the redundant memory cells and enables the user to replace a defective memory cell with a selected redundant memory cell. The field-programmable redundancy apparatus may comprise nonvolatile memory means, such as EEPROM's, to store the replacements of primary memory cells with redundant memory cells. In the reconfiguration mode, detection of a second predetermined code sequence causes the reconfiguration mode to be exited.

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